

What is claimed is:

- 1 1. A method of manufacturing a semiconductor device having a thyristor and a
2 substrate with an upper surface, the method comprising:
3 forming a thyristor having a body and a control port capacitively coupled to the
4 thyristor body, the body including an emitter region below the upper surface of the
5 semiconductor substrate; and
6 forming a conductive shunt in the substrate and extending between a node at the
7 upper surface of the substrate and the emitter region.
- 1 2. The method of claim 1, further including:
2 forming a pass device having first and second source/drain regions separated by a
3 channel region and a gate capacitively coupled to the channel region, the first
4 source/drain region being electrically coupled to the emitter region via the node at the
5 upper surface of the substrate.
- 1 3. The method of claim 2, wherein forming a conductive shunt comprises:
2 etching a trench in the substrate and adjacent to the emitter region;
3 lining the trench with an electrically insulative material; and
4 forming a conductive shunt material in the trench and electrically coupled to the
5 emitter region and to the first source/drain region.

1 4. The method of claim 3, wherein forming a thyristor having an emitter region in
2 the substrate includes implanting the emitter region via a bottom portion of the trench,
3 prior to forming the conductive material in the trench.

1 5. The method of claim 3, further including removing a portion of the liner at a
2 bottom of the trench, prior to forming the conductive material in the trench, wherein
3 forming a conductive material in the trench and electrically coupled to the emitter region
4 includes forming the conductive material electrically coupled to the emitter region via a
5 portion of the trench where the liner has been removed.

1 6. The method of claim 3, wherein etching a trench in the substrate and adjacent to
2 the emitter region includes etching a trench around a portion of the thyristor.

1 7. The method of claim 6, wherein forming a thyristor having a body and a control
2 port includes forming the control port in the trench, further including forming insulative
3 material in the trench and between the control port and the conductive shunt, the
4 insulative material being configured and arranged to electrically insulate the conductive
5 shunt from the control port.

1 8. The method of claim 3, wherein lining the trench with an electrically insulating
2 material comprises:
3 filling the trench with the electrically insulating material; and

4 removing a portion of the electrically insulating material from the trench and
5 thereby forming a lined trench.

1 9. The method of claim 8, wherein removing a portion of the electrically insulating
2 material includes exposing a portion of a bottom of the trench and wherein forming a
3 conductive material in the trench and electrically coupled to the emitter region includes
4 forming the conductive material electrically coupled to the emitter region via the exposed
5 portion of the bottom of the trench.

1 10. The method of claim 3, wherein etching the trench includes etching a trench
2 extending into the emitter region.

1 11. The method of claim 3, wherein forming a conductive material in the trench
2 includes depositing polysilicon in the trench and subsequently doping the deposited
3 polysilicon.

1 12. The method of claim 3, further including etching a shallow trench isolation (STI)
2 region in the substrate, prior to etching the trench adjacent to the emitter region, wherein
3 etching the trench adjacent to the emitter region includes etching a portion of the
4 substrate below the STI region and using said portion of the substrate below the STI
5 region to inhibit lateral diffusion of the conductive shunt material.

1 13. The method of claim 3, wherein etching a trench in the substrate and adjacent to
2 the emitter region includes etching a trench having a varied depth with a greater depth
3 below the STI region, relative to portions of the trench not below the STI region.

1 14. The method of claim 3, wherein forming a thyristor comprises:
2 forming a trench in the substrate;
3 implanting the emitter region via a bottom portion of the trench;
4 forming a first base region in a portion of the substrate adjacent to the trench and
5 electrically coupled to the emitter region;
6 forming a second base region electrically coupled to the first base region;
7 forming a second emitter region electrically coupled to the second base region;
8 and
9 forming a control port in the trench and capacitively coupled to at least one the
10 first base region and adapted to form a conductive channel between the emitter regions in
11 response to a voltage being applied thereto.

1 15. The method of claim 14, wherein forming the control port comprises:
2 forming a dielectric on a sidewall of the trench; and
3 forming the control port in the trench and capacitively coupled to at least one of
4 the first and second base regions via the dielectric.

1 16. The method of claim 15, wherein forming a trench includes forming a trench
2 around a portion of the substrate including the first base region and wherein forming the

3 control port and forming the conductive shunt includes forming the control port and the
4 conductive shunt in different portions of the same trench and electrically isolating the
5 control port from the conductive shunt.

1 17. The method of claim 1, further including out diffusing material from the
2 conductive shunt to form the emitter region.

1 18. A method of manufacturing a semiconductor device including a substrate having
2 an upper surface, the method comprising:
3 forming a vertical thyristor in the substrate, the vertical thyristor including a
4 thyristor body and a control port, the body having an N⁺ emitter region in the substrate
5 and below the upper surface, a P base region on the N⁺ emitter region, an N base region
6 on the P base region and a P⁺ emitter region on the N base region, the control port being
7 separated from the P base region by a dielectric and configured and arranged to
8 capacitively couple a signal to the P base region via the dielectric in response to a voltage
9 applied thereto for controlling current flow in the thyristor;
10 forming an N⁺ conductive shunt electrically connected to the N⁺ emitter region
11 and extending between the N⁺ emitter region and the upper surface; and
12 forming a pass device having first and second N⁺ source/drain regions separated
13 by a channel region and a gate capacitively coupled to the channel region, the first N⁺
14 source/drain region being coupled to the conductive shunt.